

FIG. 1 is a block diagram of a system 100 for dynamic code generation. The system 100 includes a transmission source 10, a receiver 20, a data sampling controller 30, a dynamic database controller 40, and a dynamic code database 50. The receiver 20, data sampling controller 30, dynamic database controller 40, and dynamic code database 50 are connected to a common bus 60. The transmission source 10 is connected to the receiver 20 via a communication link 70.

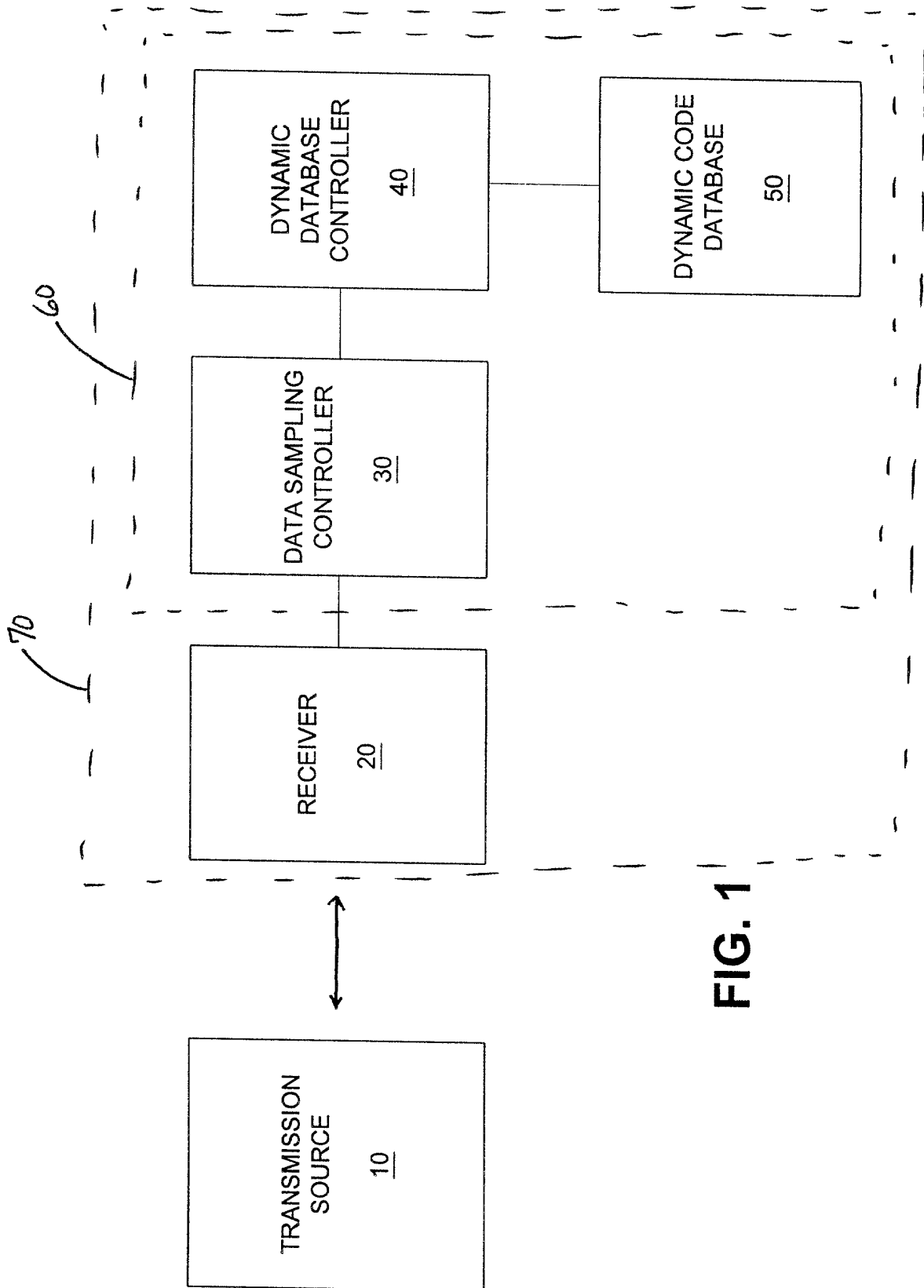


FIG. 1

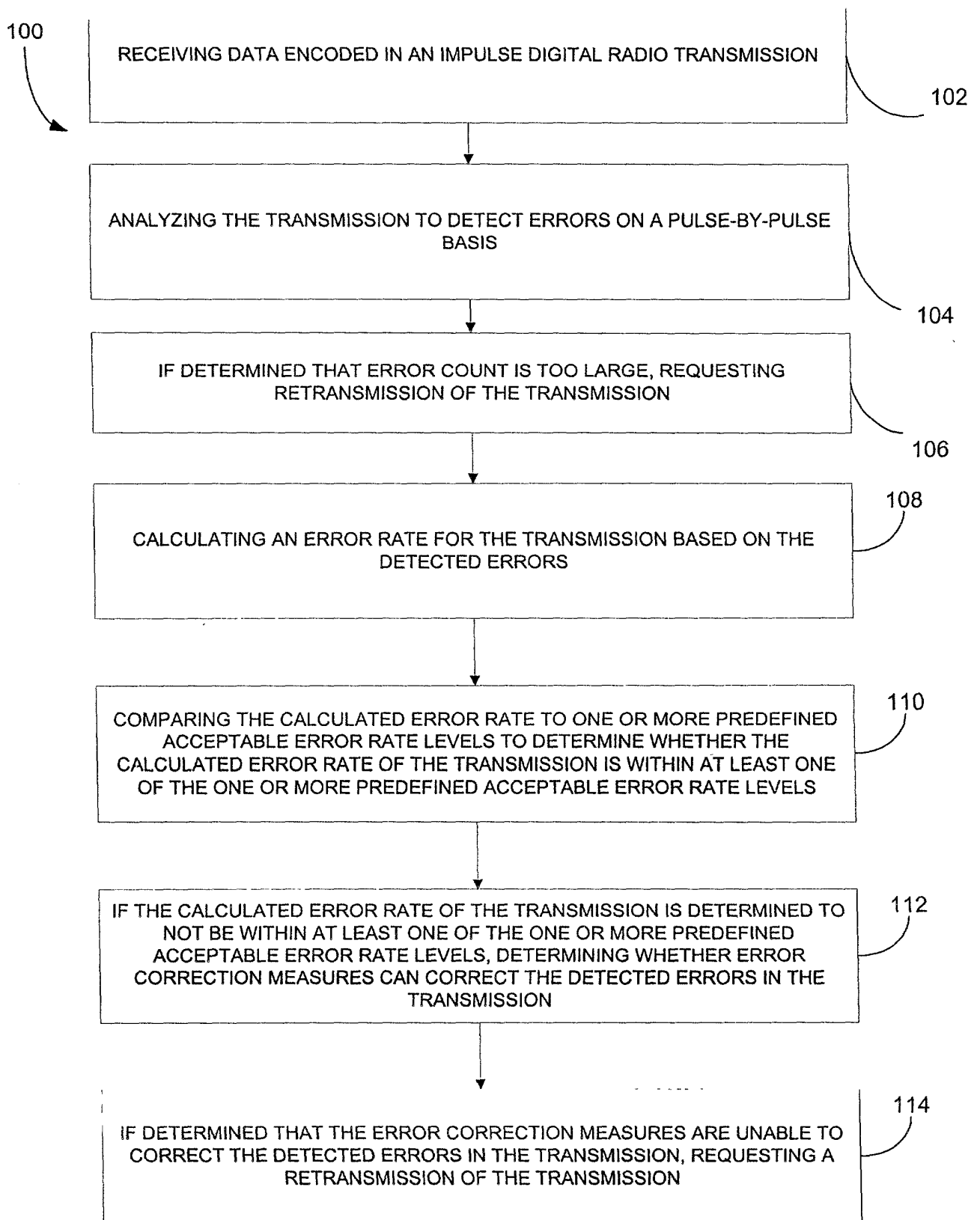


FIG. 2

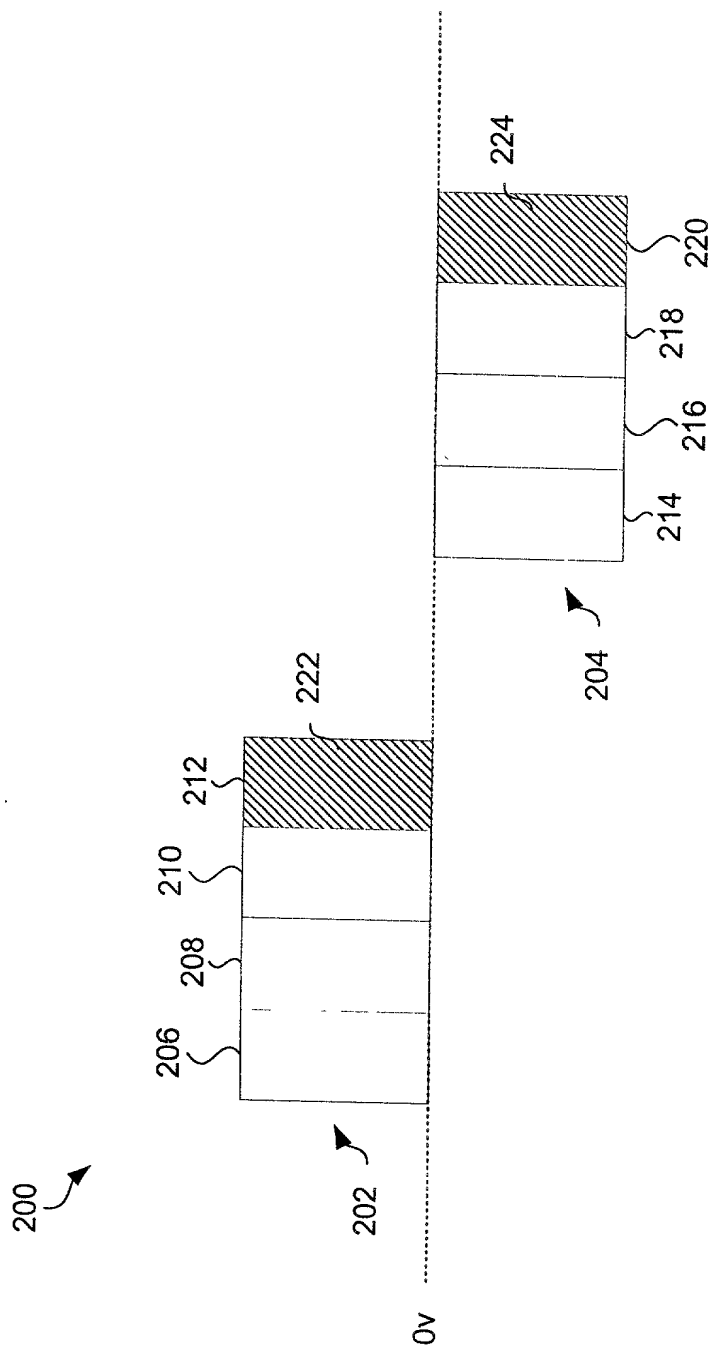


FIG. 3

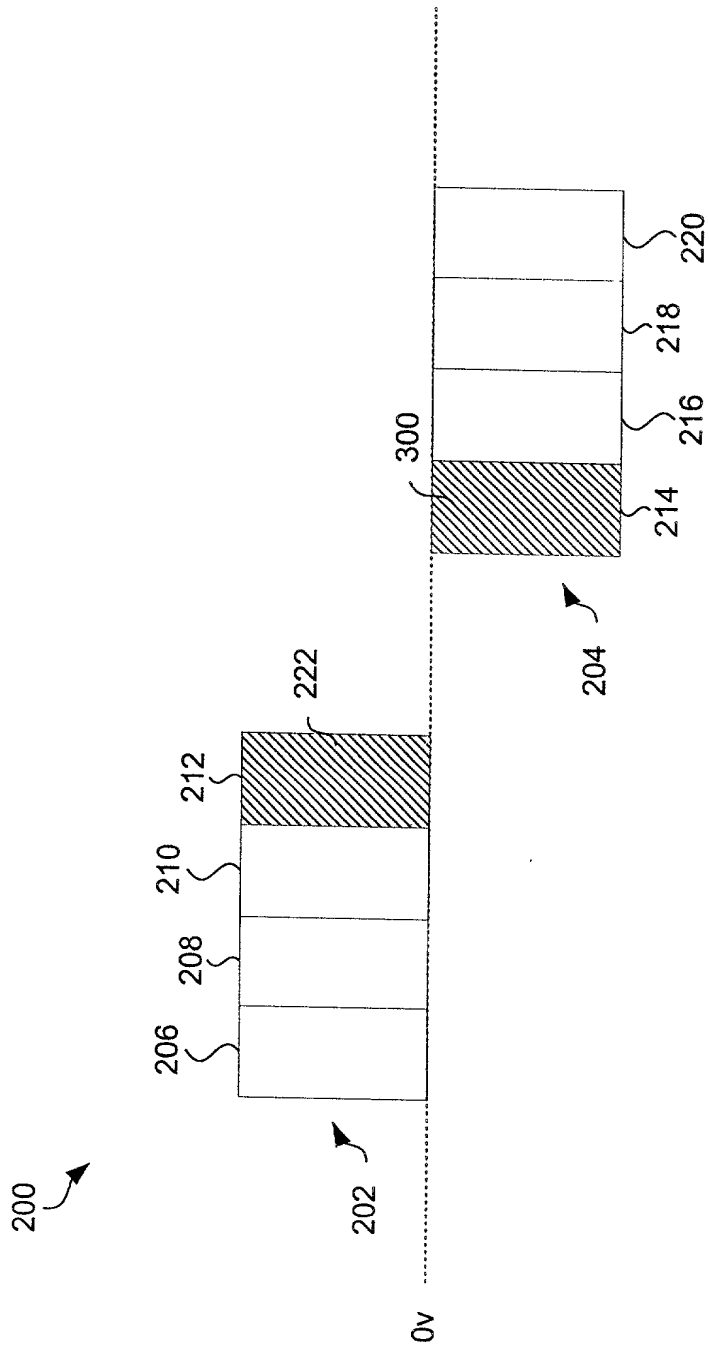


FIG. 4

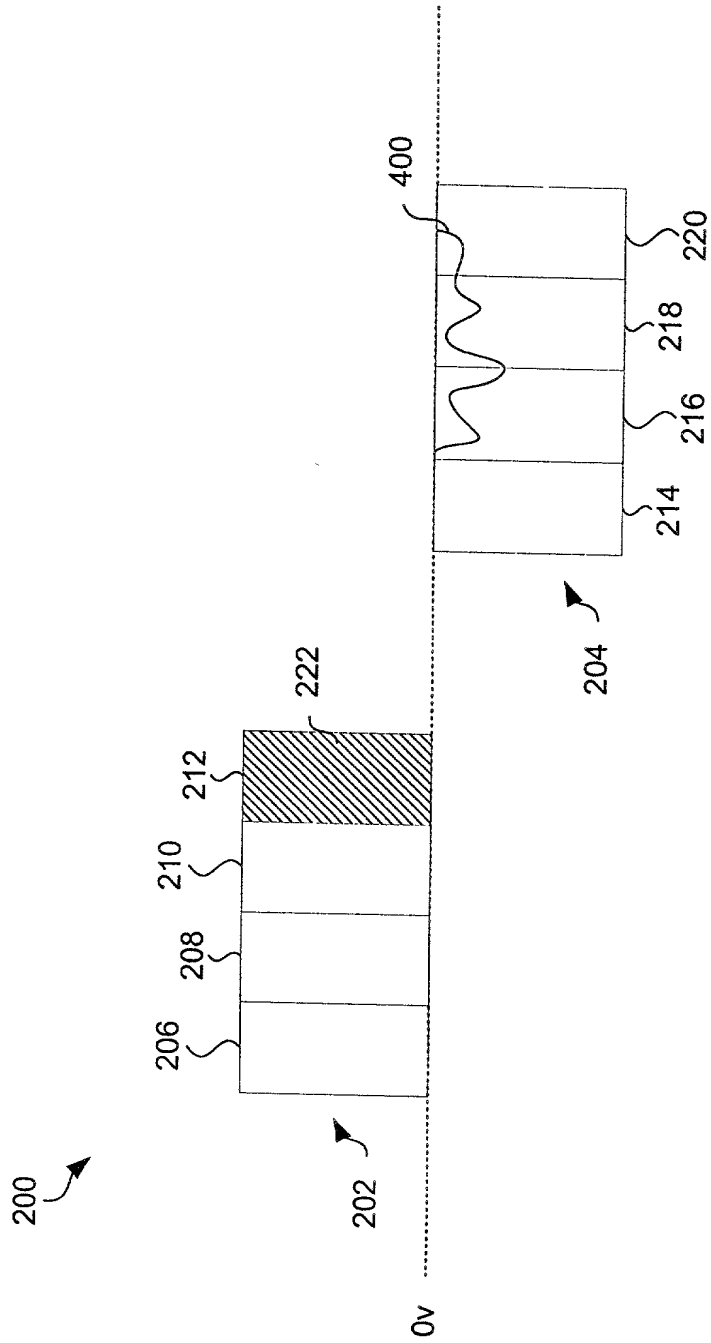


FIG. 5

FIG. 6 is a cross-sectional view of a semiconductor device 200, showing a substrate 202, a gate stack 204, and a channel layer 206. The gate stack 204 includes a gate dielectric layer 208 and a gate electrode layer 210. The channel layer 206 is disposed on the substrate 202 and under the gate stack 204. A source region 212 and a drain region 214 are formed in the substrate 202 on opposite sides of the gate stack 204. A source contact 216 and a drain contact 218 are formed on the source region 212 and the drain region 214, respectively. A top dielectric layer 220 is disposed on the channel layer 206 and the source/drain regions. A passivation layer 222 is disposed on the top dielectric layer 220. A label 500 points to the passivation layer 222.

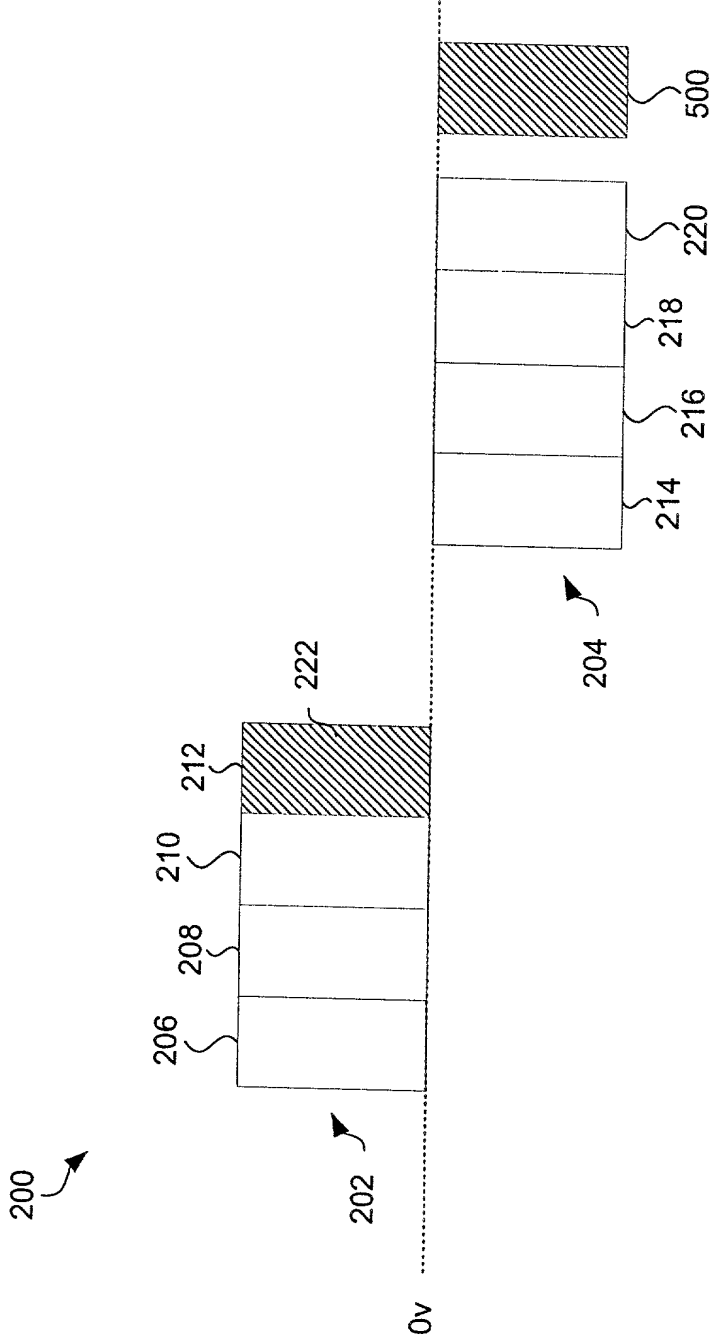


FIG. 6

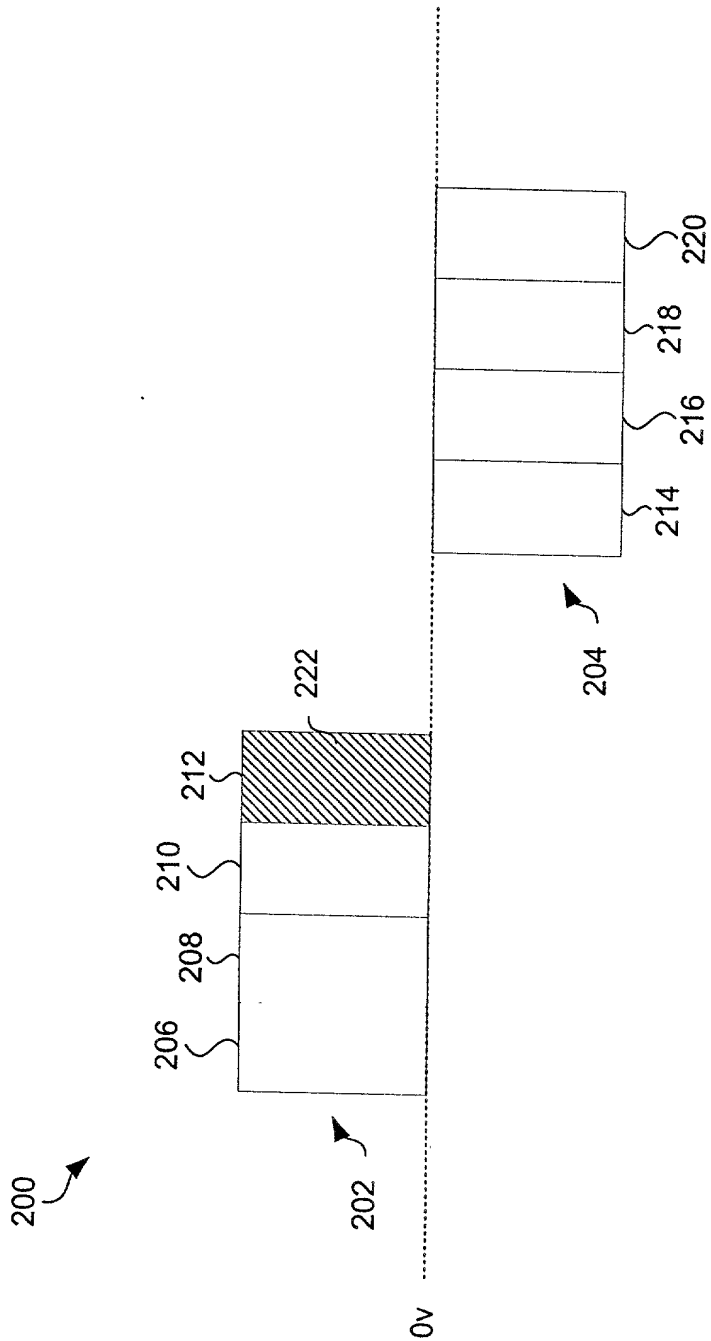


FIG. 7

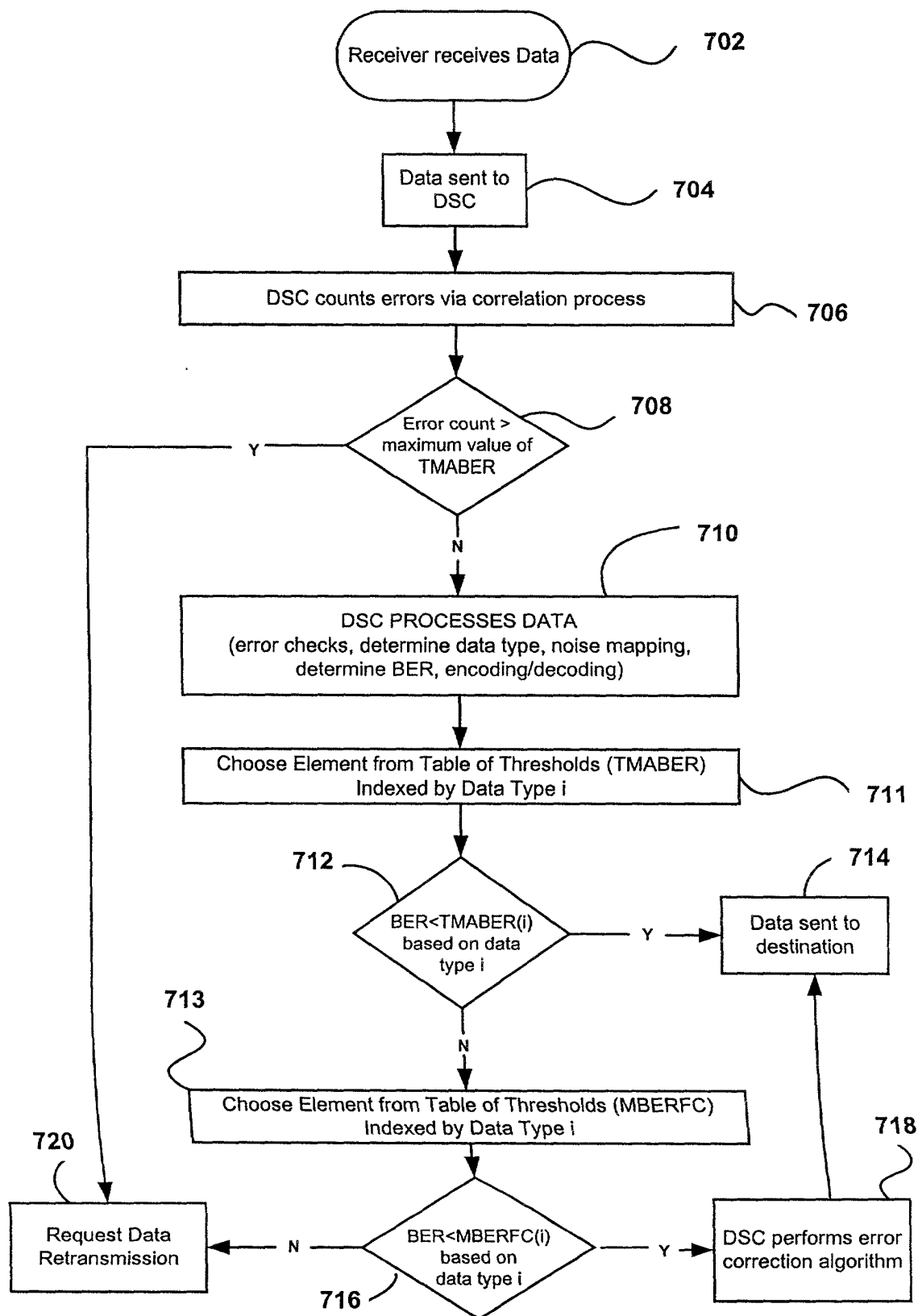


FIG. 8

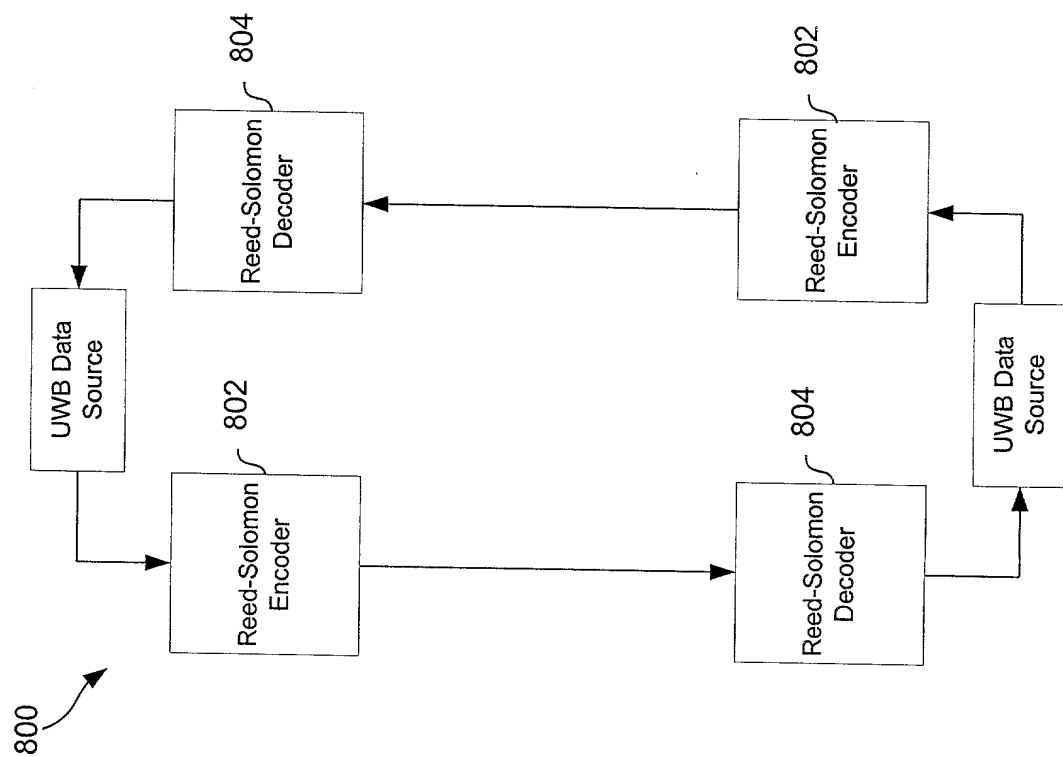


FIG. 9

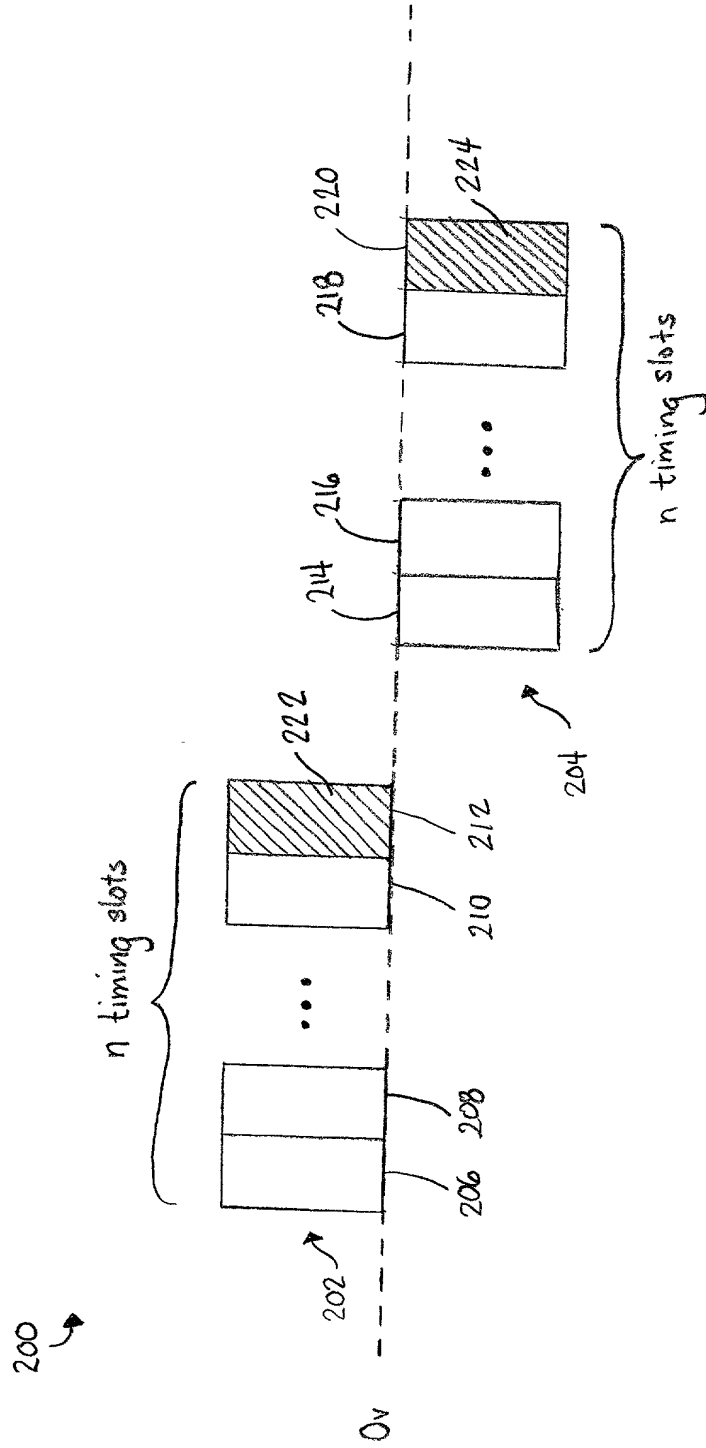


FIG. 10